

Data acquisition electronics for gamma ray emission tomography using width-modulated leading-edge discriminators



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Abstract

We present a new high-performance and low-cost approach for implementing radiation detection acquisition systems. The basic elements used are charge-integrating ADCs and a set of components encapsulated in an HDL (hardware definition language) library which makes it possible to implement several acquisition tasks such as time pickoff and coincidence detection using a new and simple trigger technique that we name WMLET (width-modulated leading-edge timing). As proof of concept, a 32-channel hybrid PET/SPECT acquisition system based on these elements was developed and tested. This demonstrator consists of a master module responsible for the generation and distribution of trigger signals, 2×16 -channel ADC cards (12-bit resolution) for data digitization and a 32-bit digital I/O PCI card for handling data transmission to a personal computer. System characteristics such as linearity, maximum transmission rates or timing resolution in coincidence mode were evaluated with test and real detector signals. Imaging capabilities of the prototype were also evaluated using different detector configurations. The performance tests showed that this implementation is able to handle data rates in excess of $600\text{k events s}^{-1}$ when acquiring simultaneously 32 channels (96-byte events). ADC channel linearity is $>98.5\%$ in energy quantification. Time resolution in PET mode for the tested configurations ranges from 3.64 ns FWHM to 7.88 ns FWHM when signals from LYSO-based detectors are used. The measured energy resolution matched the expected values for the detectors evaluated and single elements of crystal matrices can be neatly separated in the acquired flood histograms.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Over the last 5 years, we have been investigating different approaches for the implementation of combined small-animal PET/CT and SPECT/CT scanners (Vaquero *et al* 2005, 2008, Lage *et al* 2007, 2009a, 2009b). In this scenario, the aim of this work has been to provide a flexible, high-performance and low-cost hardware platform to test novel detector configurations and to implement the data acquisition system of the emission tomography scanners.

Photon detectors used for PET and SPECT produce randomly distributed bursts of fast analog signals which need to be acquired, digitized and transferred to a computer in order to extract information such as the energy deposited or the position of the interaction. Additionally, for PET applications accurate timing information of the signals (in the nanosecond range) is essential. Recent implementations faced this task by simultaneously digitizing in several channels the entire signal shape at sampling rates ranging from 40 to 80 MHz (Engels *et al* 2002, Guerra *et al* 2006, Streun *et al* 2006, Fontaine *et al* 2009). In order to achieve a more accurate time window than the resolution of the sampling frequency, the pulse starting time is normally refined by interpolating between the pulse samples. These systems process the data stream either off-line by a host computer or, more commonly, in real-time using embedded coprocessors such as DSPs or FPGAs, in which parallel and pipelined signal processing architectures are implemented. This approach makes it possible to carry out typical acquisition tasks such as trigger (Monzó *et al* 2009), time stamp (Guerra *et al* 2008), baseline restoration (Hongdi *et al* 2010), position and energy calculation (Semmaoui *et al* 2008) and coincidence sorting using advanced real-time digital signal processing techniques, without adding dead time in the process. However, a drawback of this type of implementation is its complexity and the fact that it requires significantly higher power consumption than its analog counterparts. Although the scalability and power of this approach is clear, choosing this method implies a long development time and a relatively high material cost since these systems require sufficient throughput to process data streams of several hundreds of Mbps per channel. An alternative and more conventional way of digitizing fast scintillation signals is the use of an analog approach based on either peak-sensing or charge-integrating ADCs. These implementations require external time pickoff circuits, such as constant fraction discriminators (CFD), to generate the trigger signal that initiates the acquisition of the analog signals with accurate timing resolution (Young *et al* 2000, Chiozzi *et al* 2002, Laymon *et al* 2003, Martin *et al* 2005, McElroy *et al* 2005, Wu *et al* 2009). Although this approach has been extensively applied for PET and SPECT systems, it has the drawback that it requires additional analog conditioning stages such as shaping amplifiers, baseline restorers or the aforementioned CFDs, which normally are implemented in relatively expensive ASIC devices (application-specific integrated circuits) and optimized for specific tasks and detector types (Pratte *et al* 2004, Spanoudaki *et al* 2006). In addition to the possibilities commented above, some implementations combine both architectures. One of the more promising approaches is a project called OpenPET (Moses *et al* 2009) proposed by researchers at the Lawrence Berkeley National Laboratory (CA, USA). In their initial draft, they projected a flexible architecture in which each detector signal is digitized by a continuously sampled ADC and processed in a FPGA to compute energy, interaction position and the event time. Time pickoff is carried out by means of a leading-edge discriminator which generates a timing edge that is time stamped by a TDC (time-to-digital converter) implemented inside the FPGA. OpenPET also defines some other modules in charge of different tasks such as coincidence sorting, multiplexing or data transmission to a host computer, providing a complete specification for the development of this type of system. Maybe one of the more important aspects of this specification is to be an open source, meaning that all technical data (board layout, specifications, source code, etc) will be publicly available.

Although there is a wide variety of possibilities for the implementation of radiation detectors for PET and SPECT applications (mainly based on solid-state detectors or on combinations of scintillators with photodetectors) and variations in the geometry of tomographic systems, there is a set of common requirements that makes it possible to define a specific architecture suitable for most of these applications. These main requirements are summarized as follows: to detect the instant of the interaction of the photons (which can be done using a timing signal directly obtained from each detector or e.g. as the sum of the output signals of one or various detectors), to define trigger policies to discriminate valid events (e.g. single interactions with a minimum energy deposition or coincident interactions between a predefined set of detectors), to digitize the output signals of the required detectors to obtain accurate energy and position information and to transfer the digitized data to a computer. In this work, we present and evaluate a mixed analog/digital solution which provides a simple and high-performance architecture for the development of radiation detection acquisition systems. The main elements of this architecture are (1) fast analog comparators to convert analog timing signals into the digital domain; (2) width-modulated leading-edge discriminators (WMLEDs) implemented in HDL (hardware definition language) and used to identify valid events; (3) a set of additional hardware components encapsulated in an HDL library, which implements several acquisition tasks such as generating gate signals or managing data from ADCs; and (4) charge-integrating ADC channels for the digitization of the required detector signals. As proof of concept, we used these components to implement a hybrid PET/SPECT prototype consisting of a master module responsible for the generation and distribution of trigger signals, 2×16 channel ADC cards (12-bit resolution) for data digitization and a 32-bit digital I/O PCI card (NI-6533-DIO-32HS, National Instruments Corporation, USA) for handling data transmission to the computer.

2. Materials and methods

2.1. Basic analog components

Analog components of the proposed architecture are charge-integrating ADC channels and fast comparators for pulse detection. Since the technical details of the exact design of those components are beyond the scope of this paper, we only comment here on the general guidelines followed in our implementation. ADC channels are based on the AD7482 (Analog Devices, USA); this component includes a parallel interface and is capable of providing 3 MSPS with 12-bit resolution. Each ADC channel contains a pulse-shaping amplifier to adjust the integral of detector signals to the A/D input span. Our criterion was to select a shaping time short enough to achieve high counting rates in PET mode while reducing the probability of pulse pile-up. Additionally, to ensure good stability and accurate quantification of the pulses, a previously designed closed-loop baseline restorer (BLR) was incorporated in each channel. Finally, a 50 ns analog delay line is included between the BLR output and the integrator input in order to synchronize the gate signal with the arrival of the signal to be integrated.

Single and coincidence event detection is based on ultra-fast comparators and special HDL components (WMLEDs) detailed in the following section. For each timing signal (i.e. the last dynode signal of a photomultiplier), we used two levels of comparison (U1 for comparator C1 and U2 for comparator C2, figure 1(b)) to derive a time pickoff signal. In our case, the comparators are based on the ADCMP600 chip (Analog Devices, USA), which provides a 3.5 ns propagation delay and a TTL compatible output stage. Schematic views of the ADC channels and comparators used in our implementation are shown in figures 1(a) and (b), respectively.

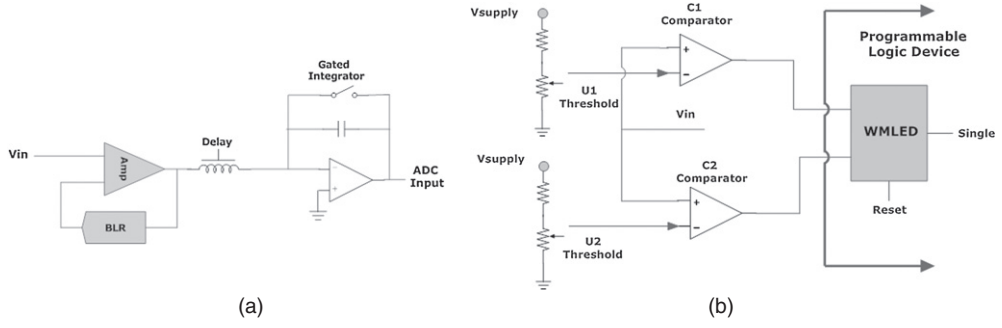


Figure 1. Basic analog components of the proposed architecture: (a) simplified block diagram of ADC channel implementation. (b) Schematic drawing of the two-level comparator included for converting analog timing signals into the digital domain. Output of comparators is directly fed into a programmable logic device or similar in which WMLED circuits are implemented.

2.2. Width-modulated leading edge timing

The design specifications for the development of this technique were to obtain a suitable event-discrimination scheme for PET and SPECT applications that also provided versatility, ease of calibration and the possibility of implementation using commercially available PLDs (programmable logic devices). For simplicity, we decided to base our implementation on leading-edge discriminator circuits which, although they have good time pickoff characteristics, have time walk when the dynamic range of the timing signals is large. That is, an input pulse with small amplitude but with the same rise time as a larger pulse will cross the threshold at a later time. Thus, the timing of the output pulse is shifted by this change in amplitude. In addition, although leading-edge discriminators or other circuits, such as constant fraction discriminators, provide a certain degree of energy discrimination based on a comparison threshold, the timing resolution of these circuits gets worse due to the time-walk effect as this threshold is raised.

The basic idea behind the width-modulated leading edge timing (WMLET) technique is to generate, in a single step, a digital timing signal with dynamic duration containing information about both the energy and timing of the detected photon. Functionally, a WMLED is a slope-to-time converter whose input signals are the output pulses from two comparators (C1 and C2, figure 1(b)), and its output is a digital pulse equivalent in length to the difference between the arrival times of the input pulses. Under these conditions, the width of the output pulse (single signal) can be defined by either of the following expressions:

$$\text{Single}_{\text{width}}(-) = T - |T_{u2} - T_{u1}| \quad (1)$$

$$\text{Single}_{\text{width}}(+) = T + |T_{u2} - T_{u1}|, \quad (2)$$

where T is a fixed value and T_{u2} and T_{u1} are the points at which the timing pulse from the detector crosses the voltage thresholds $U1$ and $U2$, respectively (figures 1 and 2). As discussed in the following paragraphs, depending on the input configuration of the WMLED, we can obtain the behavior indicated by either equation (1) or (2), which will be referred to as positive and negative configurations.

Figure 2 illustrates the operation principle of the WMLED circuits: the first row shows three fast analog pulses from a scintillation detector for PET or SPECT (identical rise times

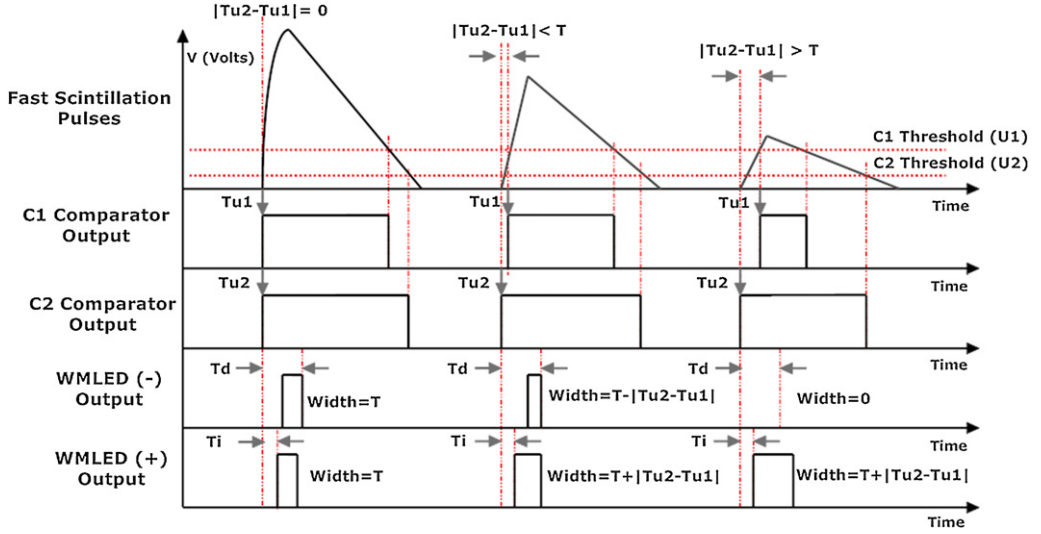


Figure 2. Width-modulated leading edge discriminator (WMLED) operation principle using the negative and the positive configurations.

but different amplitudes). The threshold values of the upper and lower level comparators (C1 \rightarrow U1, C2 \rightarrow U2) are also shown in this graph. In the same figure, the second and third rows show the signal at the output of the C1 and C2 comparators for each analog input pulse. The fourth row shows the single pulse generated for the WMLED circuit (negative configuration). For the first pulse shown in the plot, the slope tends to infinity in the comparison range and $|T_{u2} - T_{u1}|$ is 0 ns; therefore, the pulse width at the output of the WMLED is equal to T . For the following pulse $0 < |T_{u2} - T_{u1}| < T$, and the pulse width at the output of the WMLED is consequently defined by expression (1). For the last analog timing pulse of the plot, $|T_{u2} - T_{u1}|$ is greater than T and no pulse is generated at the discriminator output. Similarly, the fifth row illustrates the behavior of this technique when the positive configuration of the circuit is used. In this case, as indicated by expression (2), the output pulse width of the WMLED circuit ranges between T and $T + |T_{u2} - T_{u1}|$ as a function of the rising slope of the analog timing pulse.

Additionally, as indicated in the last rows of figure 2, there is a constant delay between T_{u2} and the falling edge of the single pulse (T_d) when the negative configuration is used, and between T_{u2} and the rising edge of the single pulse (T_i) when the positive configuration is used. The duration of those time intervals (T_d and T_i) and the T parameter can be explained using the equivalent circuits and chronograms shown in figure 3: in the negative configuration of WMLED circuits (figure 3, left), the output of the comparator with the greater comparison threshold (C1 on figures 2 and 3) is used as the clock signal for a edge-triggered D-type flip-flop with asynchronous clear, whereas the output of the comparator with the lower comparison threshold (C2) is delayed for T_{delay} and used to clear this element. As a result of this implementation, the timing parameters shown in the chronograms of figure 3 match the internal timing parameters of the flip-flop: T_{clear} is the clear time of the flip-flop and T_{co} is the delay from the rising edge of the register's clock to the time the data appear at the register output.

Using those parameters, it is possible to express the values of T_d and T as well as the working conditions of the equivalent circuit:

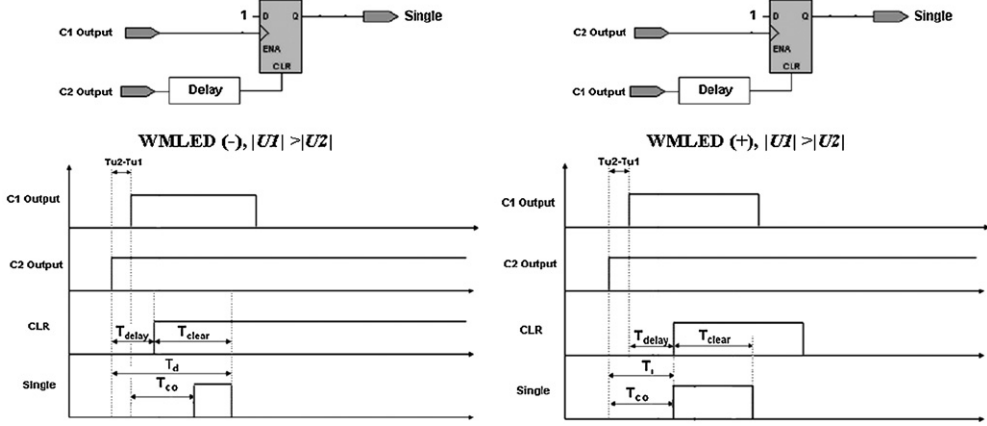


Figure 3. Simplified block diagrams for the implementation of a WMLED and internal chronogram showing the operation principle using the negative (left) and the positive (right) configuration of the WMLED circuits. Note that the change in the behavior of the circuit from positive to negative or vice versa can be achieved by interchanging the inputs or varying the threshold values $U1$ and $U2$.

$$\text{WMLED}(-) \begin{cases} T_d = T_{\text{delay}} + T_{\text{clear}} \\ T = T_d - T_{\text{co}} \\ \text{Single}_{\text{width}} = T - |T_{u2} - T_{u1}| \end{cases} \Leftrightarrow T_d > \max(T_{\text{co}}, \max|T_{u2} - T_{u1}|). \quad (3)$$

In the same manner for the positive configuration,

$$\text{WMLED}(+) \begin{cases} T_i = T_{\text{co}} \\ T = (T_{\text{delay}} + T_{\text{clear}}) - T_i \\ \text{Single}_{\text{width}} = T + |T_{u2} - T_{u1}| \end{cases} \Leftrightarrow T_i < (T_{\text{delay}} + T_{\text{clear}}). \quad (4)$$

The parameter T included in expressions (1)–(4) stands for the output pulse width of the WMLED circuit when both comparison thresholds ($U1$ and $U2$) are at the same value. This implicitly makes it possible to configure the WMLED circuit to work as a leading-edge discriminator in which, after a time T_i from the T_{u2} instant, a pulse of duration T is generated at the output.

Using either of these implementations, we can calibrate our system in order to implement different trigger policies. For example, in SPECT mode, we use the width of this pulse combined with the pulse detection circuit to discriminate pulses outside a predefined energy range. In other possible PET-mode implementations, coincidence detection is based on the logical AND function of two single signals (WMLED output signals); therefore, the coincidence resolution time for a given T can be adjusted by tuning the threshold values of the comparators. Note that, in this case, if for example the negative configuration of WMLED circuits is used together with the logical AND of single signals for coincidence detection, threshold values not only discriminate single pulses without sufficient energy but also limit maximum energy difference between coincident photons, thus providing an intrinsic scatter rejection mechanism.

Since the timing resolution and performance of this technique is a function of the specific implementation of the WMLED circuits, we decided to develop these components adapted to an appropriate programmable logic device. In this regard, we found that CPLDs such as MAX7000 and MAX3000A families (Altera Corporation, USA) or XC9500 series (Xilinx,

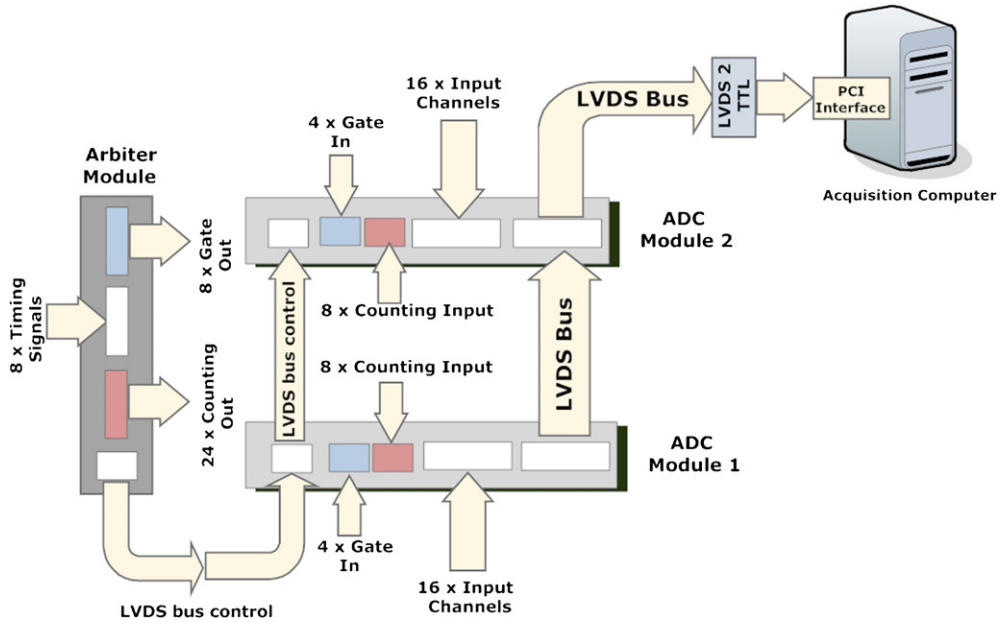


Figure 4. Components and topology of the demonstrator data acquisition system. The system contains an arbiter module, two ADC modules with 16 channels each and a PCI interface to transfer data to a computer. The ADC modules and the PCI card are connected using a 32-bit LVDS bus.

USA) were appropriate due to their simple architecture and predictable internal delays. For the implementation of the trigger system of the arbiter module, we selected the EPM3512AFI256-10 device from Altera.

In order to avoid time differences due to internal delays on the chip, we adapted our WMLED implementation to fit each component in a single macrocell of these devices. The delay component shown in both circuits of figure 3 was implemented in our case, adding the necessary glue logic to force the related signal to pass through an internal stage of the CPLD with appropriate delay. In the resulting implementation, the parameters used in expressions (1)–(4) can be derived from the timing model and internal timing parameters of a particular device, thus making it possible to obtain a wide range of timing properties either by varying the implementation or by changing the device. In our case, we used an implementation providing a T value of roughly 4 ns.

2.3. Data acquisition system prototype

We split the functionality of the DAQ system into two different hardware modules (figure 4), partially following the architecture defined in Hack *et al* (1986) and sharing similarities with the system detailed in Proffitt *et al* (2005, 2006). The main module is an arbiter used for detecting single or coincident photons, which generates counting and gate signals for the ADC modules. These ADCs (two identical modules are present in this system) are intended for acquiring the position signals from the detectors, as well as data transmission to a computer. Additionally, we included two general-purpose 12-bit counters for each 4-channel set (8 counters in total for each ADC module). These are transmitted with each digitized event. The ADC cards and the digital I/O PCI interface are connected using a high-speed 32-bit

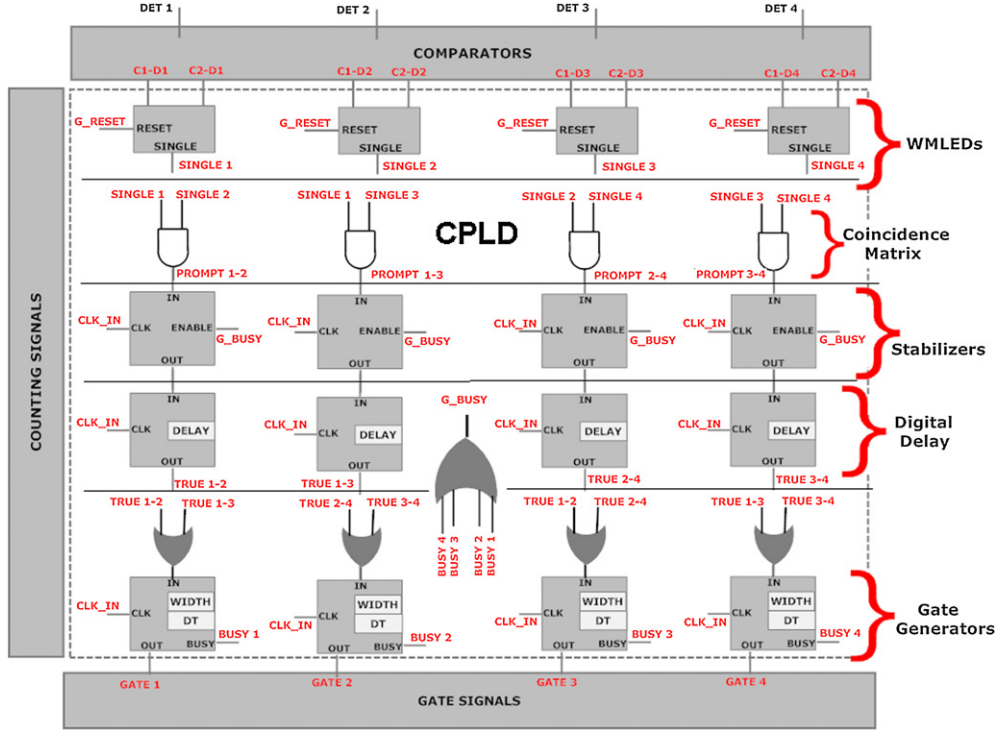


Figure 5. Arbitrer module of the VrPET data acquisition system (PET mode implementation). The input signals to this module are fast analog timing signals. Output signals are the gate signals used to operate the ADC modules and general-purpose counting signals. These latter signals are not shown in the drawing, because in the real implementation, they are obtained using the intermediate signals and some glue logic.

LVDS bus. Each ADC channel and counter includes a 4-bit header that serves as an identifier for the data frame analysis.

The arbitrer module is designed to connect up to eight detectors that can be configured to work in single mode (SPECT) or in coincidence mode (PET). The expected input signals (timing signals in figure 4) are fast pulses from radiation detectors. Each of these signals is fed into a two-discriminator input stage that generates signals for the corresponding WMLED. In order to improve the timing resolution for PET applications, the lower discriminator threshold is the same for all the detectors. Figure 5 shows a simplified design developed with our library of HDL components and used in the VrPET system (Lage *et al* 2009a). This scanner uses two opposing detector modules, each of them comprising two single detectors. Each single detector is able to accept coincident photons with its two opposing detectors. As shown in figures 5, for each single detector (DET1 to DET4), permissible coincidences (DET1-DET2, DET1-DET3, DET2-DET4 and DET3-DET4) are defined by the user by means of glue logic, designated as a *coincidence matrix* in the chart. The output signals of the coincidence matrix are fed into a group of components that we call *stabilizers*. These components are designed to accept input signals with a minimum duration of roughly 2.0 ns (used in our tests). It is also possible to configure these components to accept input signals with a maximum duration, if needed. As with WMLED components, other implementations make it possible to obtain different timing properties. Additionally, since the acquisition of an event has a non-zero

dead time, the stabilizer components have an enabling input which disables the output of the component when its corresponding ADC module processes a previous event or when another ADC module uses the LVDS bus (see the G.BUSY signal in figure 5). When a valid event is detected (pulse with a maximum or minimum width), the corresponding stabilizer component produces a pulse of fixed duration at its output that is passed to the following stage. Because of the concept used in this system, it is necessary to delay the position signals with respect to the timing signals in order to synchronize the gate signal for the ADC modules with the arrival of position signals. In this context, the *digital delay* components (shown in figure 5) synchronize gate generation with the arrival of the signals to be integrated. These elements contain an unsigned integer literal in their specification (DELAY) that defines the number of clock cycles that the output signal will be delayed by. Finally, the output of the digital delay components feeds the input of the *gate generator*-type components, in which two unsigned integer literal values must be defined: WIDTH refers to the length in clock cycles of the gate signal (integration window width) and DT refers to the dead time in clock cycles of the corresponding ADC module for the integration, acquisition, conversion and transmission of the data event (for CLK_IN signals shown in figure 5, we used a 100 MHz clock signal). The behavior of this component is rather straightforward: when a pulse is received at its input, a gate signal with a length predefined by WIDTH and the clock frequency is generated at its output. Additionally, a signal of DT cycles duration is generated at the BUSY output of this component in order to disable the associated *stabilizer* components during the processing of the current event. For the implementation of a SPECT system called rSPECT (Lage *et al* 2009b), we used the same components shown in figure 5 with no glue logic acting as a coincidence matrix. The counting signals shown in figures 4 and 5 are obtained from either the logic function 'AND' or the logic function 'OR' of some intermediate signals of the CPLD (such as *true* or *prompt* signals shown in figure 5) and directly connected to the counters present on the ADC cards.

Each ADC module contain 16 channels (12 bit per channel) whose internal topology groups the channels in sets of 4 with an independent gate input for each of them. These ADC boards are prepared to work almost independently since they only need the gate signal to start the data acquisition, conversion and transmission. A set of switches has been included in the ADC boards to configure the number of ADC channels triggered per event, making it possible to configure these boards for 4 channels per detector (up to 4 independent detectors connected to each card) or 16 channels per detector (1 detector per ADC card). The ADC firmware consists of a finite states machine (FSM) to trigger data conversion and digital data read-out, and a communication module that serves as an interface with the acquisition computer. When any ADC card receives a gate signal from the arbiter module, the FSM starts its procedure. When conversion finishes, digitized data together with the counter values contained in the ADC cards are passed to the output interface and sent to the PC via the LVDS bus using a burst handshaking protocol. Because of the possibility of using more than one ADC card per event or receiving simultaneous events from different ADC cards, we included unidirectional daisy-chain arbitration for the LVDS bus access control (LVDS bus control lines of figure 4). The management scheme is based on a specific token-ring architecture in which, for each detected event, the token (generated by the arbiter module and sent to the first ADC card of the chain) passes through all the ADC cards. If the card needs to put data on the bus, the token is held until it finishes the data transmission and passed to the following card in order to repeat the operation if necessary. The total time required by a single card to digitize an event and send it to the computer (T_{ADC}) is defined in expressions (5) and (6):

$$T_{\text{ADC}}(\text{ns}) = T_{\text{Int}} + T_{\text{Conv}} + T_{\text{trans}}, \quad (5)$$

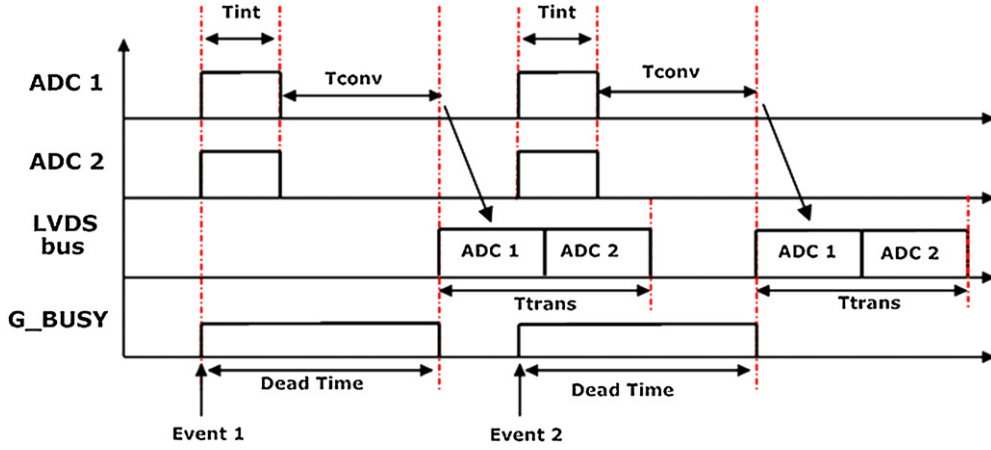


Figure 6. Example timing diagram showing the data transmission protocol of the system working in PET mode. ADC1 and ADC2 refer to the facts taking place in each ADC module of the system, LVDS bus indicates the data flow in the bus and G_BUSY refers to the BUSY signal of one of the corresponding gate generator components of the arbiter module (figure 5).

$$T_{\text{trans}}(\text{ns}) = T_{\text{CLK}} \times \frac{(\text{Counters} + \text{Channels})}{2}, \quad (6)$$

where T_{int} is the integration time of the signals (ns), T_{conv} is the conversion time of the ADC chip (300 ns for the AD7482) and T_{trans} is the time required to transmit the digitized data and the counters to the PC. As indicated in equation (6), T_{trans} depends on the period of the signal used for the data transmission ($T_{\text{clk}} = 50$ ns in our current implementation) and the number of *Channels* and *Counters* included in the event, divided by 2 because data words are sent in pairs for the LVDS bus. Self-locking of each ADC card is controlled by the BUSY signal of its corresponding *gate generator* component (see figure 5). In our current implementation, the *DT* literal value of this component is set to be equal to

$$\text{MAX}(T_{\text{Int}} + T_{\text{Conv}}, T_{\text{trans}}). \quad (7)$$

This makes it possible to pipeline the data digitization (integration plus conversion stages) with the data transmission, thus reducing ADC dead time. Figure 6 illustrates an example of a chronogram of this procedure assuming that $T_{\text{int}} + T_{\text{conv}} > T_{\text{trans}}$ and that the system works in coincidence mode with two detectors, each of them connected to an ADC module (ADC1 and ADC2). After the detection of a valid coincidence, the arbiter sends the gate signal to both ADC modules (duration equal to T_{int}) and, when the integration of the signals finishes, the ADC chips carry out the conversion procedure (duration equal to T_{conv}). After data read-out from the ADCs to the CPLD, the ADC1 module puts the digitized data and the corresponding counters in the LVDS bus and passes the token to the following ADC module, which does the same (there is a 100 ns overhead between data from both ADC modules due to the token transmission that has not been included in the diagram). During integration and data conversion, the BUSY signal of the corresponding *gate generator* (figure 5) remains active, thus ensuring that no other events will be sent to these ADCs while the current event is being processed.

Table 1. Detector configurations used in the performance evaluation

| Detector configuration number | Scintillator ^a / dimensions (mm ³) | Photo-detector type | Number of position signals | Gate width (ns) |
|-------------------------------|---|---------------------|----------------------------|-----------------|
| 1 | NaI(Tl)/ $1.4 \times 1.4 \times 6$ | H-8500 | 16 | 320 |
| 2 | LYSO/ $1.5 \times 1.5 \times 12$ | H-8500 | 4 | 120 |
| 3 | LYSO/ $1.5 \times 1.5 \times 12$ | H-8500 | 16 | 120 |
| 4 | LYSO/ $1.5 \times 1.5 \times 12$ | SiPMT | 4 | 230 |

^a Scintillator crystals combined with the H-8500 PS-PMT are pixelated matrices of 28×28 elements.

For configuration 4, we used a 4×4 pixelated matrix.

2.4. Performance evaluation

We checked the performance of the demonstrator data acquisition system in terms of maximum acquisition rate, linearity of the input channels, timing resolution in PET mode and quality of energy spectrum and position profiles acquired in single and in coincidence modes. We also tested the effect of using different scintillation materials (pixelated matrices of LYSO and NaI (Tl)) and photo-detectors (position sensitive photomultipliers and a MPPC-33-2 \times 2-50 5900 SiPM array) and the effect of changing the resistor network of the read-out electronics (4 or 16 position signals) on system performance. The detector configurations are summarized in table 1. The following subsections detail the system setup and performance measurements carried out for each experiment.

2.4.1. Pedestals and linearity of input channels. The pedestal values of the system were evaluated for the 32 channels by acquiring at different integration window lengths (from 40 to 640 ns). In this case, a 10 kHz square signal was doubled and fed into two WMLEDs configured in such a way as to trigger the 32-channel acquisition at each pulse of the square signal (as in the example shown in figure 6). For each integration window, values acquired in each channel were histogrammed and the resulting peaks were fitted to Gaussian functions. Plots of peak channel position versus integration window width were used to measure the pedestals of input channels, and the FWHM of these peaks was used to determine the effect of this systematic error. Additionally, the spectra of ^{22}Na (511 keV and 1.27 MeV emissions) and $^{99\text{m}}\text{Tc}$ (140 keV emission) sources were acquired (10^{10} counts). These two sources with different energies make it possible to test the linearity of the DAQ in a realistic experimental setting. To acquire the energy spectra, we used the detector 1 configuration (table 1). The energy information was obtained as the sum of the values of all the acquired position signals.

2.4.2. Maximum acquisition rates. The maximum acquisition rates of the DAQ were determined by using both periodic test signals and real signals from detectors. For measurements with test signals, we used a laboratory generator to obtain a periodic square wave with appropriate amplitude and variable frequency. We doubled the signal and fed them into two WMLEDs configured to detect coincident photons. In this test, two complete ADC modules (16 channels plus 8 counters per ADC module) were acquired for each event (96 byte events). Although the theoretical dead time is $1.2 \mu\text{s}$ (calculated using expression (7)) with this configuration, we set a DT value equal to $1.5 \mu\text{s}$ literally corresponding to the gate

generator components, in order to compensate the overhead caused by the daisy chain and to ensure that the PCI interface data throughput (roughly 500 Mbps when configured in burst mode) was not exceeded during the tests. The acquisition software used in this experiment processed the data frames to locate valid events (based on the header information), subtract pedestals, extract the position signals and counter values and save the valid events to disk in LIST mode. Since the data are directly transferred to the acquisition software without any intermediate storing media, such as FIFO memories, data frames must be processed in real time, thus adding an additional dead time source. The effect of this processing has also been quantified by enabling and disabling the write-to-disk procedure on the software, which proved to be the most restrictive task after profiling the source code.

Since events are not periodic but randomly distributed, the rates obtained in this test are only indicative of the theoretical performance. In a second assessment stage, we obtained measurements with real signals from two radiation detectors (configuration 1, table 1). These detectors were configured with a symmetric charge division circuit (Olcott *et al* 2005) providing 16 position signals and a timing signal obtained from the last dynode of the photomultiplier (properly shaped). The timing signals were fed into two WMLEDs and position signals of each detector were fed to one of the two ADC modules present on the system. All of the eight available counters were sent with each data event. As in the latter case, we set the *DT* literal value of the associated gate generator components equal to $1.5\ \mu\text{s}$, to allow a direct comparison between both experiments. Additionally, and given that the detectors in this test were configured in SPECT mode, the processing of new events during simultaneous processing of other events was blocked, thus maintaining coherence in bus access. The detectors were exposed to different concentrations of $^{99\text{m}}\text{Tc}$ and the recorded count rate versus activity on the FOV was plotted. In this experiment, all the software processing including the write-to-disk procedure was enabled.

2.4.3. Timing resolution in PET mode. Timing resolution in PET mode was measured using two opposing detectors (configuration 3, table 1) with an encapsulated ^{22}Na source between them. Timing signals from detectors were fed into two WMLED circuits, which were configured to implement the negative, positive and LED configurations. The rise time of the timing signals was 15–18 ns with an amplitude dynamic range from 0 to roughly 1.1 V. For tests with the positive and negative WMLED configurations, the lower comparison threshold was set at 65 mV while the upper threshold was set at 140 mV for both detectors. Working in LED mode, both comparison thresholds were set at 65 mV. Timing resolution was determined by measuring the histogram of time differences between coincidence events. The resulting peaks were fitted to Gaussian functions and time resolution calculated as its FWHM. These time differences were obtained in all the experiments with calibrated cable delays. No correction for time mis-alignment of signals between individual detectors was applied.

2.4.4. Position profiles and energy resolution. For these experiments, data were acquired in single mode using a ^{22}Na -encapsulated source. Pixels of the field flood histograms were positioned using a weighted mean position calculation algorithm involving all the digitized signals for each event (4 or 16). The resulting position values were mapped to individual crystals by means of a previously computed lookup table (LUT), and the energy value for each event was histogrammed on the corresponding crystal spectrum. For each configuration, we report on the average peak-to-valley ratio of the position profiles and the energy resolution at 511 keV. The energy performance was calculated for each crystal by fitting the channels

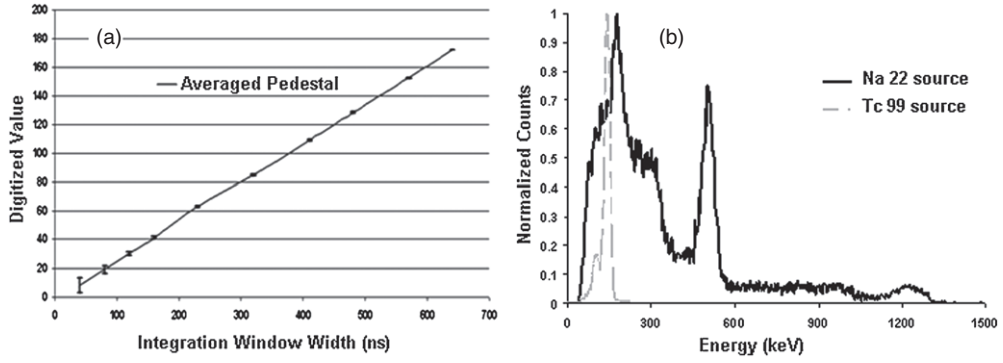


Figure 7. (a) Averaged pedestal value of the 32 channels for different integration window widths. (b) Energy spectra of a single NaI(Tl) crystal irradiated with a ^{22}Na source and with a ^{99}Tc source.

near the photopeak to a Gaussian function. The energy resolution was then calculated as the FWHM of the Gaussian function divided by the photopeak energy as a percentage.

3. Results

3.1. Pedestals and linearity of input channels

Figure 7(a) shows the average pedestal value for the 32 channels as a function of the integration window width. The error bars indicate the average FWHM of the pedestal value for the 32 channels with each integration window width. As expected, this average FWHM is reduced with the integration width, leading to less than one-channel width when a window greater than 120 ns is used.

The energy spectra of a single NaI(Tl) crystal irradiated with ^{22}Na and $^{99\text{m}}\text{Tc}$ sources are also shown in figure 7(b). The spectra clearly show the photopeaks of the ^{22}Na source at 511 and 1275 keV as well as the 140 keV photopeak of the $^{99\text{m}}\text{Tc}$ source; a prominent backscatter peak (~ 200 keV) due to the detector enclosure and shielding used during the experiment is also visible in the ^{22}Na spectrum. Comparison of the different peak positions (140, 511 and 1275 keV) shows that ADC channel linearity is better than 98.5% in energy quantification.

3.2. Maximum acquisition rates

Figure 8(a) shows the results obtained with the signal generator. The behavior of the system when no write-to-disk operations are performed by the PC is almost as theoretically expected, providing a peak processing rate of 647 kcps when the test signal delivered 669 kcps. When the write-to-disk procedure is enabled in the software, the recorded count rate shows a significant increase in dead time at roughly 400 kcps and a peak acquisition rate at 492 kcps when the test signal provides 650 kcps (%dead time = 24.3%).

Using real signals from detectors, a maximum count rate of 362 kcps was obtained with 312 μCi within the FOV. Figure 8(b) represents the combined acquisition rate of the two detectors. Differences in instantaneous count rate between detectors during the test were lower than 2.5%. In this case the graph shows the inter-locking effect present in the system due to the use of the same transmission medium (LVDS bus) to transfer ADC-card data to the PC.

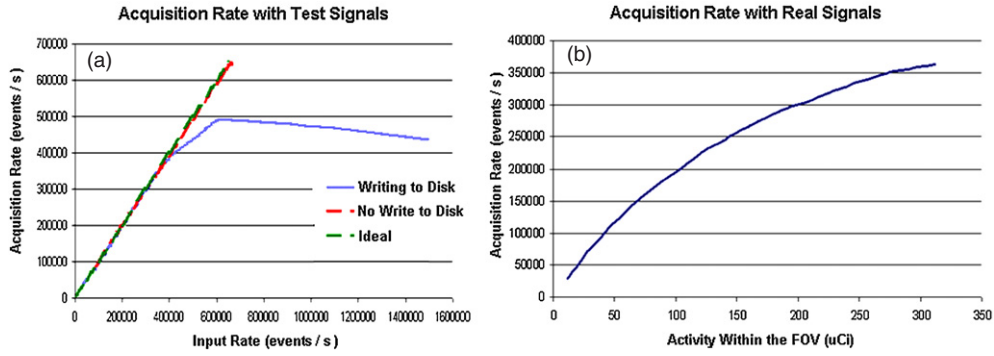


Figure 8. Measured acquisition rates when periodic test signals were used (a) and when real signals from radiation detectors were used (b).

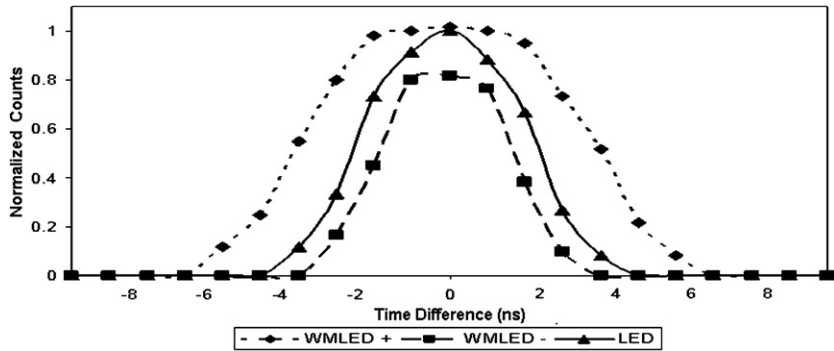


Figure 9. Timing resolution (Gaussian fit) for different configurations: WMLED (+), WMLED (−) and LED. Number of counts is normalized at the maximum value obtained using leading-edge discriminators.

3.3. Timing resolution in PET mode

The results obtained in these tests are summarized in figure 9. Timing resolution when positive WMLED configuration was used is 7.88 ns FWHM (11.6 ns FWTM). For the negative WMLED configuration, the timing resolution is 3.64 ns FWHM (6.65 ns FWTM). In the last case when WMLEDs were configured as leading-edge discriminators, the timing resolution was 4.66 ns FWHM (8.77 FWTM).

When positive WMLED configuration was used, the total number of events detected was 64% greater than with the leading-edge discriminator. This increment is due to the fact that, in this case, coincidence events with greater time walk were accepted as valid events. Using the negative WMLED configuration, the total number of detected events was 30.2% lower than with the leading-edge discriminator. In this latter case, only coincident events with energy level higher than a certain value (above the lower comparison threshold) and similar energies between them were accepted as valid events.

Since the timing resolution using WMLEDs is a function of the threshold values, the rise time of the signals and the WMLED implementation/configuration, the reported values are only indicative of the performance of this system using these settings. In general, in order to

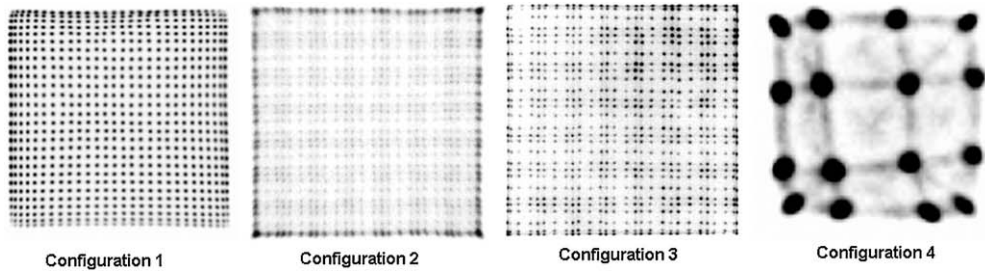


Figure 10. Flood field histograms obtained for each of the configurations summarized in table 1.

obtain the best timing resolution, one must set the lower level threshold above the noise level (worst case with these detectors $45 \text{ mV} \pm 10 \text{ mV}$) and as low as possible to reduce errors due to time walk.

3.4. Position profiles and energy resolution

Figure 10 shows the field flood histogram obtained for each of the configurations summarized in table 1. For configuration 1, the 28×28 crystals are clearly separated and the average peak-to-valley ratio of the image is better than 25:1; energy resolution for the 511 keV photopeak is 13.8% on average for the entire detector. Using the second configuration, only 26×26 crystals are clearly resolved in the image (outer crystals are not resolved). The average peak-to-valley ratio in this case is 2.4:1 (for the 26×26 central crystals); energy resolution at 511 keV is 19.4% on average for the entire detector. With the third configuration we obtained an average peak-to-valley ratio of 7.4:1. Due to the use of 16 signals instead of 4 (we only changed the electronics from configuration 2 to 3), outer crystals can now be resolved and energy resolution improves to 16.2%. Finally, for the SiPM-based configuration, we obtained an average peak-to-valley ratio better than 10:1. In this case, average energy resolution for the entire detector was 15.8%. Additional details about the experimental settings of this detector can be found in España *et al* (2008).

4. Discussion and conclusions

We presented a new and simple trigger technique (WMLET) and constructed a demonstrator acquisition system based on it. When used for coincidence detection, WMLED circuits make it possible to easily adjust coincidence time resolution, thus providing a simple and versatile interface for the implementation of different trigger policies. Additionally, if coincidences are detected using the logic function AND of the WMLED circuit outputs, the maximum energy difference between both photons could be limited online. When used for single event applications, our technique makes it possible to detect and discriminate events as a function of their energy in a single stage. The simplicity of the trigger system (based on potentiometers) enables us to vary dynamically the WMLED configuration. For example, with the positive configuration, it is possible to enhance sensitivity at low counting rates or adapt the coincidence time window to the characteristic of the input signals. With the negative configuration, it is also possible to improve time resolution, thus reducing the system dead time at high counting rates. Another advantage is that the use of the rising edge of the timing pulses makes it possible to

implement pile-up rejection strategies based on the length and shape of the comparator outputs without adding dead time.

Although the implementation evaluated does not improve the timing performance of current technology, mainly based on CFD circuits capable of providing sub-nanosecond time resolution (Moszynski *et al* 2006) with fast scintillators (such as LYSO or LSO), it enables a significant cost reduction when compared with other implementations (the total manufacturing cost of the system presented including electronic components, PCB fabrication and the PCI interface is less than 5000 Euros). Additionally, as mentioned above, it is possible to obtain better timing performance by changing the device or changing the WMLED implementation and/or its configuration. For example, when assessed with a 10 kHz signal from a pulse generator (Model 417, Phillips Scientific, USA) providing a constant pulse with a rise time of 1.5 ns, 6 ns width and 800 mV amplitude, we obtained a timing resolution of 1.32 ns FWHM (3.52 ns FWTM) using the negative WMLED configuration. In addition, in this work we proposed and used CPLDs implemented on 0.30 μm CMOS technology because scheming uniformity and predictability of the delays make the implementation simpler than if the current generation of devices (such as the Altera MAX II family) were used. In these newer PLDs, logic elements are more complicated and a wider range of implementations (with different timing properties) for the same HDL component is possible. In this case, care must be taken to avoid differences in timing properties, e.g. due to different internal delays on the chip or different implementations of the same component inside the PLD.

Although the demonstrator system presented in this work is functional, we did not exploit all its possibilities in our implementation, because of the use of a shared transmission medium (LVDS bus) as an output interface. This implies that the processing of new events must be blocked during simultaneous processing of other events. Future prototypes will include on each ADC module an independent transmission medium such as a USB or an Ethernet interface to better separate data acquisition and transmission tasks. A preferred implementation consists of adding an Ethernet-based output to each ADC card and using the LVDS bus (with fewer lines) only to stamp coincident events. All the Ethernet outputs can be plugged in a Gigabit Ethernet switch in charge of sending the data to one or various acquisition computers. This should reduce the dead time of each detector to less than 500 ns per event, greatly improving the throughput and overall performance of the system. Another drawback of this prototype is the large number of data transferred to the computer during acquisitions and the increase in dead time caused by the processing on the PC side. A possible solution could be to move energy and position calculation to a hardware device, thus reducing in this way the number of bytes necessary for event characterization, as well as the processing overhead in the computer. Another solution could be the use of a more powerful PCI interface with internal memory in order to eliminate the dead time caused by the write-to-disk procedure. In any case, adding improvements to the system will increase the overall material cost and complexity, so the cost-effectiveness could be reduced compared with other approaches.

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